Open access Journal International journal of Emerging Trends in Science and Technology

A Survey on Different Topologies, Switching Techniques and Routing Algorithms for A Network on Chip

Authors
Neetu Soni[1], Khemraj Deshmukh[2]

[1] Deparment of Electronics and Telecommunication,CSVTU,Bhilai,C.G.,India
Email: *neetu.soni29@email.com*
[2]Deparment of Electronics and Telecommunication,CSVTU,Bhilai,C.G.,India
Email: *khemraj.deshmukh@gmail.com*

Abstract
Network on Chip (NoC) is a new paradigm for making interconnections within System on Chip (SoC) system. With the increasing chip integration and decreasing feature size the SoC does not meet the challenges of the new process technologies .The challenges include complexity and increased delay in communication and also the bus contention and arbitration slows down the data movement which degrades the overall performance of Soc. Noc is a design platform that can meet these challenges to a great extend. In the network design of the NoC the most essential things are a network topology and a routing algorithm. Routers route the packets based on the algorithm that they use. In this paper a study of the different routing algorithms for network on chip is presented that can cope up with above mentioned problems arising in SoC. The routing algorithm of a given NoC system is measured with respect to performance metrics such as latency, throughput and load distribution. Here we are about to deal with the different topologies ,switching techniques ,performance analysis of NoC routing algorithms such as XY routing algorithm, OE routing algorithm and DyAD routing algorithm .
keywords- *NoC , Routers, routing algorithms, latency, throughput, XY ,OE , DyAD*

1. INTRODUCTION

In the early 1990s ,the resources or the processing components have been integrated into a single silicon chip ,this paradigm was known as System On Chip (SoC).It used topologies based on shared buses and point-to-point links for communication but with the growing silicon technology, they are becoming too costly for this purpose because of their complexity, poor scalability, and increase delay in communication and also the bus contention and arbitration slows down the data movement and unpredictable performance, and high power consumption [1][2][3].To overcome these problems Networks-on-Chip (NoC) was proposed by Dally and Towles [4] which used packet-switched communication providing not only high degree of scalability, but also ensures reuse of communication architecture [3]. In the network design of the NoC the most essential things are a network topology and a routing algorithm. Routers route the packets based on the algorithm that they use. In this paper, we present the details of different routing algorithms for NoC design approach. such as XY routing algorithm, OE routing algorithm and DyAD routing algorithm in section 2.The performance parameters in evaluating NoC designs and routing algorithms are throughput and average packet delay and the load distributions[5][6][7]. In the NoC architecture, the chip consists of a set of interconnected nodes where each node can be a general-purpose processor like a Digital Signal Processing commonly known as processing element (PE). Within each node a router is embedded in order to connect it to its neighbouring nodes. The router consists of four ports: West, East,

South and North ,to connect with other routers and a local port to connect with PE .

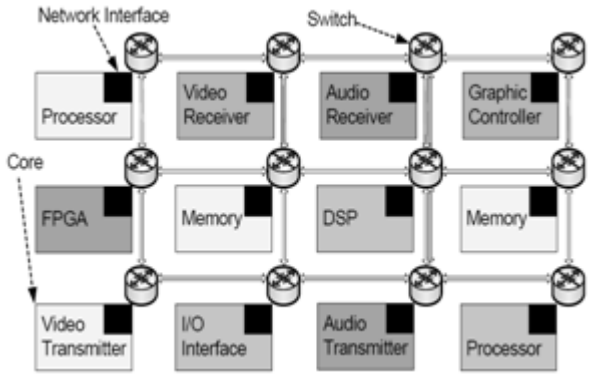

Figure.1. Noc Architecture

It means a router has five inputs and five outputs, as shown in figure.2[9]. Router consist of Routing algorithm and switching techniques, where routing algorithm defines as the path taken by a packet between the source and the destination and switching techniques defines how and when to connect their inputs to outputs and also determines the time taken by the message to transfer along these path. The overall performance of a NoC depends on parameters such as topology, routing algorithm, flow control, and switching technique [9] .

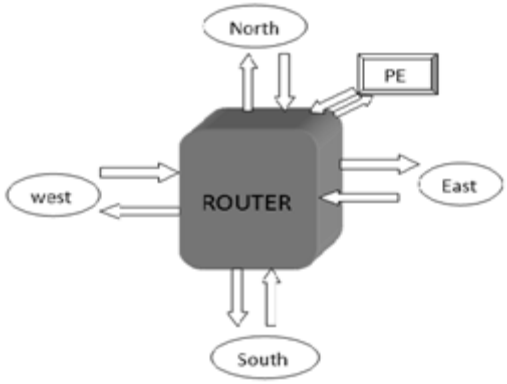

Figure.2. Structure of a Router

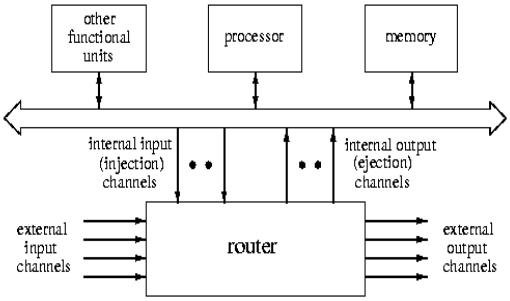

Figure.3.Generic structure of a processing node

In section 2 we give an overview of the topologies, routing algorithms and switching techniques used within the NoC.

2. Overview Of Topologies, Switching Techniques And Routing Algorithms

2.1. Topologies

Topology describes how nodes are connected and placed in a network, affecting the bandwidth and latency of a network. There are different topologies such as mesh ,torus, butterfly star, and polygon topology. 2D mesh and torus are the most common topologies due to their grid-type shapes and regular structure which are the best suited for the 2D layout on a chip.

Mesh. It consists of m columns and n rows. In the intersection of two wires the routers are situated and the computational resources are near routers. X-Y coordinates define the addresses of routers and resources. Mesh topology is easy to implement as all nodes are in equally distance as shown in Figure.4 and also makes addressing of the cores quite simple during routing. A mesh topology has four inputs and four outputs from/to other routers, and another input and output from/to the PE.

Torus. A torus network is a mesh network in which the heads of the columns and the tails of the columns interconnected and the left sides of the rows are connected to its right sides. Torus network has better path diversity than mesh network, and it also has more minimal routes.

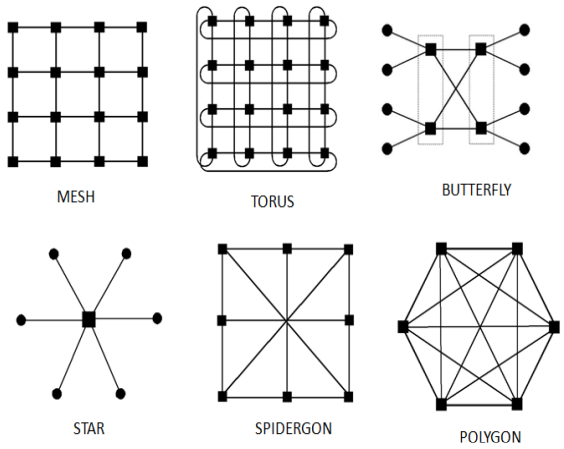

Figure.4 .Types of Topologies

Star. It consists of a router in the middle of the star, and computational resources or sub-networks at the ends of the star network. Central router requires quite large capacity because all the traffic

between the ends resources goes through the central router. It has the congestion problem in the middle of the star.

Butterfly. It is butterfly-shaped network may be unidirectional or bidirectional, typically uses a deterministic routing. A simple unidirectional butterfly network contains equal and separate input ports and output ports and several router levels in between. Packets coming to the input ports on the left side of the network are forwarded to the desired output on its right side [14]. Whereas in a bidirectional butterfly network, all the inputs and outputs are on the same side of the network. Packets coming to inputs are first routed to the other side of the network, then turned around and routed back to the correct output.

Polygon. This is a circular network where packets move in loop from router to other. Network becomes more diverse when chords are added to the circle. In spidergon network the chords are only between opposite routers.

2.2. Switching Techniques

Switching techniques define the way and time of connections between input and output ports inside a switch.

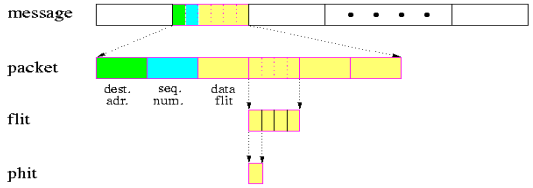

Figure.5. Communication units

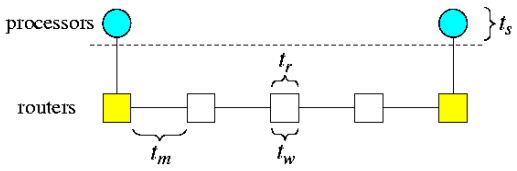

Figure.6. General time model of a conflict-free communication between distant nodes.

There are several switching techniques, such as Circuit Switching, Packet Switching and Wormhole Switching. We will use the following notation in this section and throughout the rest of this course:

- w = flit size = phit size = channel width (in bits),
- M = packet size (in flits),
- t_r = time of routing decision within one router during building a routing path (in seconds),
- t_w = intra-router switching latency once the router has made the routing decision and a path has been set up through the router (in seconds/phit),
- $t_m = 1/B$ = inter-router channel latency (in seconds/flit). The transmission latency of a packet of M flits between two adjacent routers is Mt_m seconds.
- d = the length of a routing path.

2.2.1. Circuit Switching

In circuit switching [5] the physical path between the source and destination is reserved during data transmission. The header flit is injected into the network which contains the destination address and some control information and moves toward the destination through intermediate routers reserving physical links it has passed. When it reaches the destination, the followed path gets reserved and the acknowledgement is sent back to the source. This path can be released by the destination or by the last bits of message itself.

Base communication latency in this switching technique:

A message of length M transmitted to distance d takes time

$$t_{CS}=d(t_r+(p+1)(t_w+t_m))+Mt_m$$

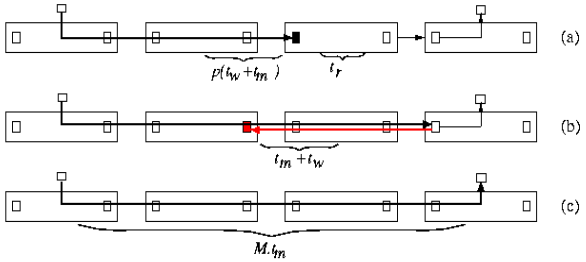

Figure.7. Circuit switching on a path of length (a) The probe progresses towards the destination router. (b) The acknowledgment is sent back to the source. (c) The whole message is transmitted along established circuit using its full bandwidth.

The probe needs time $d(t_r+p(t_w+t_d))$ to get to the destination, the acknowledgment takes $d(t_w+t_d)$ to get back, and the data transmission takes Mt_m. This technique is useful when the messages are infrequent and long. As it reserves the entire path

it may block other messages causing unnecessary delays.

2.2.2.Packet Switching

This is alternatively known as store and forward switching. In this switching technique, the message is divided into fixed-length data blocks, called packets. Each packet is routed individually from source to destination and each packet has a packet header containing all routing and control information, which enables intermediate routers to find the packet's destination. Thus, the latency of a packet depends and changes accordingly with the distance between source and destination. The latency increases with the increase in distance between source and destination.

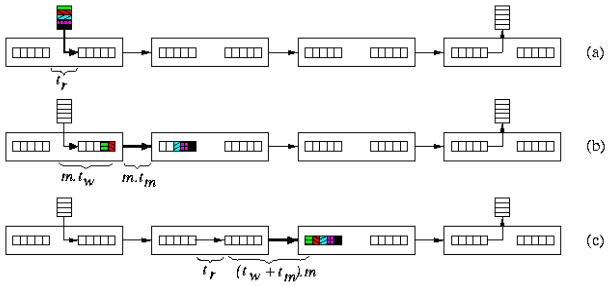

Figure.8. Store-and-forward switching of a packet. (a) Routing decision is being made in the first router. (b) The packet is performing the first hop to the second router after has been copied to the output buffer of the first router. (c) The whole packet after the second hop.

Base communication latency in this switching technique:

A packet of length M transmitted to distance d takes time

$t_{ps}=d(t_r+(t_w+t_m)M)$

At every router, routing decisions must be made and then the packet hops to the next router, which takes $t_r+(t_w+t_m)M$, and this repeats d times.

Packet switching is useful when messages are short and frequent and utilizes the whole communication link , while the circuit switching may keep the reserved path idle for some time. However ,if packet size becomes large ,the storage requirements at the individual routers can enhance and multiple packets has to be buffered at a node.

2.2.3.Wormhole Switching

In this switching technique [5] the message is divided into data flits in order to compress the buffer size at routers and achieve routing much faster. The input and output buffers of a router are large enough to contain a few flits.

In the network ,a message is sent at flit level in pipelined fashion. The header flit contains the information about routing and reserves a path in the network for other flits following it. In case of blocking wormhole switching simply stops every flit in its current position to collect the following data and requires smaller buffer size. When a message is blocked it occupies several routers in the constructed path and buffers a few flits at a router. which reduces average message latency. In this technique, only the header flit contains the routing information and all the incoming data flit moves along the same output channel as the preceding data flit, and the message crosses the whole channel before another message uses it making the wormhole technique deadlock prone. This risk deadlock can be solved by multiplexing several virtual ports to one physical port, in order to decrease the possibility of traffic congestion and blocking [12].

As already mentioned, we cannot mix flits of different packets into one buffer (= one physical channel), since flits carry no identity flags. However, with adding some control logic, we can split one physical channel into several virtual channels. They will have their own buffers, but will share (time-multiplex) one single physical channel medium (similarly to processes with own contexts sharing one physical processor). The total communication latency of this technique

$t_{WH}=t_s+dt_d+Mt_m$

where $t_d=t_r+t_w$.

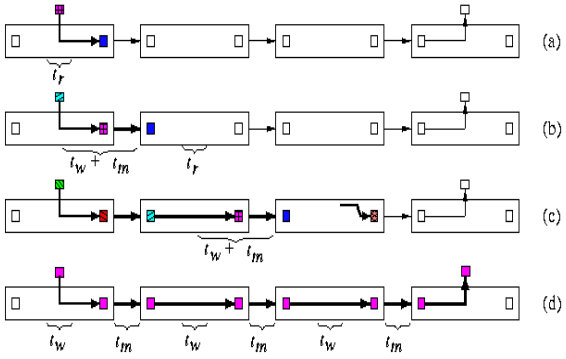

Figure.9. Wormhole switching of a packet. (a) The header is copied in the output buffer after having done routing decision. (b) The header flit is transferred to the second router and other flits are following it. (c) The header flit arrived into a router with busy output channel and the whole chain of flits along the path got stalled, blocking all its channels. (d) Pipeline of flits in case of conflict-free routing, establishing the wormhole across routers.

Wormhole routing allows simple, small, cheap, and fast routers. Wormhole mode needs less memory than the two other modes because only one flit has to be stored at once. Here the latency is smaller and a risk of deadlock is larger.

2.3. Routing Algorithms

In NoC, routing is to connect the various resources efficiently .This requires selection of not only shortest but a path that can balance the load traffic efficiently. There are many routing algorithms with some advantages and disadvantages.[13].The algorithms are classified into two : Deterministic algorithms and Adaptive algorithms .

In Deterministic Routing Algorithms [5] the same fixed and shortest routing path is always generated between a given pair of source and destination. It needs only the addresses of current and destination nodes to compute the path. As the path is fixed for the same source and destination ,message travel always along the same path and cannot use alternative paths if it encounters any blocked channels. It uses greedy algorithm that chooses always the shortest path .This routing is simple and fast when traffic is uniform. In case of non uniform traffic deterministic routing degrades in terms of latency and throughput is very poor [5].

In Adaptive Routing Algorithms ,a message is not restricted to a single fixed path but it is free in making decision for changing the route according to current network conditions while travelling from the source to the destination. It makes routing more flexible and avoids time delays, provides better fault tolerance. This algorithms has two main functions: routing and selection.Routing function provides a set of desired output channels based on the current node and destination node, Selection function finds the best free output channel from that set so that messages can take alternative route is instead of waiting for a busy channel. It also has backtracking technique, through which we can backtrack and release the previously reserved channels and thus systematically search appropriate path which is not possible in deterministic algorithms as the message will follow the same path again if we backtrack it. Adaptive routing algorithms provides flexibility but increases the complexity of hardware and makes it slower.

The other types of routing algorithms are:

2.3.1. XY routing algorithm

XY routing is a dimension order routing in which packets are routed first in x- or horizontal direction to the correct column and then in y- or vertical direction to the receiver. XY routing suits well on a network using mesh or torus topology. XY-coordinates indicate the addresses of the routers.

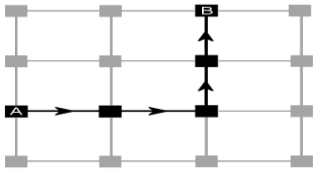

Figure.10. XY routing from router A to B

In XY routing deadlock or livelock conditions are never found. [14].
XY routing suffers some problems like when the traffic does not spread regularly over the whole network because the algorithm causes the biggest load in the middle of the network. There is a need for algorithms which equalize the traffic load over the whole network.

Pseudo Adaptive XY Routing.

Pseudo adaptive XY routing is both deterministic or adaptive depending on the condition of the network. Algorithm is deterministic when the network is not or only slightly congested .The algorithm becomes adaptive when network becomes blocked and searches routes that are not congested. This algorithm uses mesh topology in which every router has five bidirectional ports: north, south, east, west and local. The four ports north, south, east, west connect to other routers and the local port connect to the processing elements. Each port has a small buffer and a 2-bit identifier called quantized load value which tells to other routers whether the router is congested and cannot accept new packets. Packets are assigned from north having highest priority, then south, east and at last packets incoming from west have the lowest priority. In the pseudo adaptive algorithm the traffic is divided more equally over the whole network. [14]

Surrounding XY Routing.

In Surrounding XY routing (*S-XY*), there are three different routing modes. *N-XY* (*Normal XY*) mode which is same as the basic XY routing.

This mode is followed till the network is not blocked and meet any inactive routers.

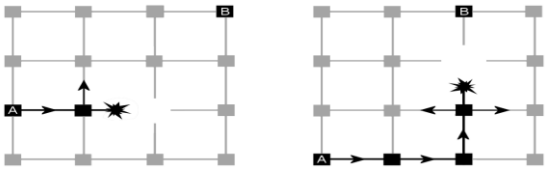

Figure .11. Surrounding XY routing in SH- XY and SV-XY modes.

SH-XY (Surround horizontal XY) mode is followed when the router's left or right neighbour is not activated. The third mode SV-XY (Surround vertical XY) is used when the upper or lower neighbour of the router is inactive. This algorithm moves the packets around the inactive routers along the shortest possible path.

2.3.2.OE Routing Algorithm

It is a distributed adaptive routing algorithm ,based on odd-even turn model [8]. It has some limitation, for avoiding and preventing from deadlock appearance. Odd-even turn model facilitates deadlock-free routing in two-dimensional (2D) meshes with no virtual channels. In a two-dimension mesh with dimensions X*Y each node is identified by its coordinate (x, y). In this model, a column is denoted the term even if its x dimension element is even numerical column and is called odd if its x dimension element is an odd number. When there is a 90-degree change of travelling direction a turn occurs

There can be eight types of turns, according to the travelling directions of the associated channels. When a change

of direction from East to South takes place it is called an ES turn. Similarly, the other seven types of turns, namely EN, WS, WN, SE, SW,NE, and NW turns. There are two main theorems in odd-even algorithm:

Theorem1:

NO packet is permitted to do EN turn in each node which is located on an even column. Also, No packet is permitted to do NW turn in each node that is located on an odd column.[8]

Theorem 2:

NO packet is permitted to do ES turn in each node that is in an even column. Also, no packet is permitted to do SW turn in each node which is in an odd column.[8]

2.3.3. Dynamically Adaptive and Determini- stic Routing algorithm

Dynamically Adaptive and Deterministic Routing algorithm (DyAD) is a routing technique which judiciously switches between deterministic and adaptive routing based on the network congestion conditions. When it switches to deterministic routing it will give low latency. When it switches to adaptive routing, it avoids congested links by exploring new routing paths as a result it will lead to higher network throughput.

3. Performance Parameter

The performance of the routing algorithms can be analyzed on the grounds of some performance parameters such as Network latency, throughput, total power consumption etc.

Network Latency is measured from the time its head flits is measured by the source to the time is consumed by the destination.

Average N/w Latency(L_{avg})=

$$\frac{1}{N}\sum_{i=1....N}\left(\frac{1}{N_i}\sum_{\forall j} L_{ij}\right)$$

where

i=1 to N and for all value of i

L_{ij}=packet latency of packet j

N_i =No. of packet received by processor i

N= No. of processors in the platform

Network throughput is defined as the rate at which the network can successfully accept and deliver the injected packets.

Average N/w Throughput=

$$\frac{1}{N(T_{sim} - T_{warm})}\sum_{i=1....N} N_i$$

where

T_{sim}=Simulation time

T_{warm}=Warm up time(time before traffic generation begins)

4. Comparison between the Algorithms

The overall average latency per channel for all the algorithms such as XY routing algorithms, OE routing algorithms and DyAD routing algorithms increases with the increase in load (data packets).The average latency per channel for the XY routing algorithms is very high. The OE routing algorithms has lower average latency per channel then XY routing algorithms and the

DyAD routing algorithms have the least latency per channel .At higher load, DyAD routing algorithms shows the better results by having much less latency than other algorithms.

The average throughput of the algorithms also increases with the increase in load. The DyAD routing algorithms have the highest throughput .The OE routing algorithms have better throughput than XY algorithms but less than DyAD algorithms.

The power consumption of the algorithms also increases with the increase in the load. The OE algorithms consumes the highest network power and the XY algorithms consumes less power than OE routing algorithms. The DyAD routing algorithms have least power consumption and proves better for higher loads than any other algorithms discussed above.

5. RESULT

We studied different topologies and found that mesh and torus are the popular and easy in its implementation .Among the switching techniques Wormhole switching allows simple, small, cheap, and fast routers. Wormhole mode needs less memory than the two other modes because only one flit has to be stored at once. In this latency is smaller and a risk of deadlock is larger. We find that among the three routing techniques discussed above ,the DyAD is routing technique is the which judiciously switches between deterministic and adaptive routing based on network congestion's conditions. The XY routing technique is deterministic has greater latency and its throughput decreases with load and the OE routing technique is adaptive technique with good throughput and lower latency but has highest power consumption . In the DyAD routing technique,when it switches to deterministic routing it will give low latency. When it switches to adaptive routing, it avoids congested links by exploring new routing paths as a result it will lead to higher network throughput.

6. CONCLUSION

A different type of routing algorithm is used in different network condition. The selection of routing algorithm totally depends upon the application and the traffic of packet in the network. As simplicity in implementation is important in all architecture so an XY routing algorithm widely used . For fewer congestion and collisions Pesudo Routing Algorithm is preferred. The OE routing algorithm achieves better balance in load distribution as well as provide deadlock-free and livelock-free facility. We can't compromised with accuracy of received data , we go for the fault-tolerant routing like DyAD .If application is focused on network resources utilization the Deterministic and Adaptive routing algorithm is best choice. Finally we can say that choice of routing algorithm is totally depends upon environmental condition of NOC architecture.

REFERENCES

[1] **A. Jantsch and H. Tenhunen.** *Networks on Chip*. s.l. : Kluwer Academic Publishers, 2003.

[2] **P. P. Pandeet al.** Performance evaluation and design trade-offs for network-onchip interconnect architectures. *IEEE Transactions on Computers*. August 2005, Vol. 54, 8, pp. 1025-1040.

[3] **J. Henkel, W. Wolf, S. Chakradhar.** On-chip networks: a scalable, communication-centric embedded system design paradigm. *Proceedings of 17th International Conference on VLSI Design*. 2004, pp. 845-851.

[4] **W. J. Dally and B. Towles. 2001, Route packets**, not wires: On-chip interconnection networks.

[5] **J. Duato, S. Yalamanchili, L. Ni.** *Interconnection Networks: an Engineering Approach*. s.l. : Morgan Kauffman, 2002.

[6] **D. Seo, A. Ali, W.-T. Lim, N. Rafique.** Near-optimal worst-case throughput routing for two-dimensional mesh networks. *Proceedings of 32nd International Symposium on Computer Architecture, 2005. ISCA '05*. pp. 432 - 443.

[7] **E. B. Jung, H. W. Cho, N. Park, and Y. H. Song.** SONA: An on-chip network for scalable interconnection of AMBA-based IPs. *International Conference on Computational Science*. May 2006, Vol. 3994, pp. 244-251.

[8] **Wang Zhang, Ligang Hou, Jinhui ang, Shuqin Geng, Wuchen Wu**, 2011, Comparison Research between XY and Odd-Even Routing Algorithm of a 2-dimension 3X3 Mesh Topology Network-on-Chip.

[9] **G. Acsia, V. Catania, M. Palesi, D. Patti.** 2008 A New Selection Strategy for on-Chip Networks.

[10] **E. Salminen, A. Kulmala, and Timo D. Hamalainen**, 2008, Survey of network-on-Chip proposals.

[11] **Yuan-Long Jeang, Tzuu-shaang Wey, Hung-Yu Wang, Chung-Wei Hung, and Ji-Hong Liu**, 2000. An Adaptive Routing Algorithm for Mesh-Tree Architecture in Network-on-Chip Designs.

[12] **E. Rijpkema, K. Goossens, P. Wielage**: *A Router Architecture for Networkson Silicon*. Proceedings of Progress 2001, 2ndWorkshop on Embedded Systems.

[13] **Rantala, V., T. Lehtonen, J. Plosila,** 2006. "Network on Chip *Evaluation of Pseudo Adaptive XY Routing Using an Object OrientedModel for NOC*. Routing Algorithms", TUCS Technical Report, pp. 779.

[14] **M. Dehyadgari, M. Nickray, A. Afzali-kusha, Z. Navabi**: The 17th International Conference on Microelectronics, 13–15 December 2005.

[15] **W.J. Dally, B. Towles**: *Principles and Practices of Interconnection Networks*. Morgan Kaufmann, 2004.