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Design of Power Efficient Double Edge Triggered DLL Clock Generator

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ABSTRACT
Low power is a big concern for any electronic device in the modern world. The Delay Locked Loop (DLL) clock generators play a vital role in clock generator circuits, due to the low jitter accumulation and stability in the output. The proposed Double Edge Triggering (DET) for DLL clock generators reduces the power consumption on the clock network. The DLL is designed using single phase clocking scheme which minimizes the delay deviation and phase errors. The clock generator is designed to operate at a frequency of 500MHZ. The analysis is made between single edge triggered DLL and double edge triggered DLL and the power consumed is found to be 5.328mW and 3.43mW respectively using 65nm CMOS process.
Keywords- *Delay Deviations, Double Edge Triggered (DET), Phase Error, Self Calibration.*

1.INTRODUCTION

Low power consuming devices are of greater demand in this digital world. Portable applications use battery powered system which has limited amount of energy saving capacity. The limited amount of energy introduces the problem of power consumption. Energy efficiency is a key point for high computational devices, which include processors, web phones etc. Power consumption by the clock network in a computing systems, often constitutes the dominant portion of the total power consumption [10]. As a result, power dissipation in clock network has been the focus of many research during recent years. The clocking system consumes one third of the total power of a chip, it takes into account the clock generation and distribution as well as the structure of latches and flip flops.

Digital circuits employing clock based design generally require clock generator circuits. The most commonly used clock generators are Delay Locked Loop (DLL) and Phase Locked Loop (PLL). The main advantage of DLL clock generator over PLL is that it has the control over set up and hold time of the clock and they can be used for high speed communications[3]. The delay locked loop cancels out the input output buffer delay variations. Moreover DLL is a stable first order system with less design complexities. In addition to this PLL suffers from jitter accumulation due to the use of voltage controlled oscillator (VCO)[5]. There are two types of DLL clock generators analog and digital. Analog DLL has a better jitter performance compared with digital. [8]. This paper proposes a Double Edge Triggered (DET) DLL clock generator which samples the delay difference on both the positive and negative edges of the clock. It has an advantage that the lock speed is increased with the same stability as compared to conventional Single Edge Triggered (SET) DLL clock generator. Section II describes the architecture of the proposed double edge triggered DLL clock generator. The simulation results are shown in section III. The results of the power consumed by SET DLL and DET-DLL are analyzed in section IV.

2. ARCHITECTURE OF DOUBLE EDGE TRIGGERED DLL CLOCK GENERATOR

The architecture of DET-DLL consists of a voltage controlled delay line (VCDL), phase detector (PD), charge pump (CP) and RC filter. The structure of the proposed DLL is shown in Fig.1. The DET-DLL triggers at both positive and negative edges of the clock. For high speed operations, this technique reduces the frequency to half while it maintains the same throughput. The input clock signal is given to the voltage controlled delay line which adds a variable amount of sample delay to the input signal. Unlike a voltage controlled oscillator it does not add noise to the input signal.

The delayed clock pulse is give to the phase detector which generates a signal that represents the difference in phase between the input clock and delayed signal from VCDL. They are give to the charge pump to reduce the phase offset and the filter removes the unwanted distortions at the output.

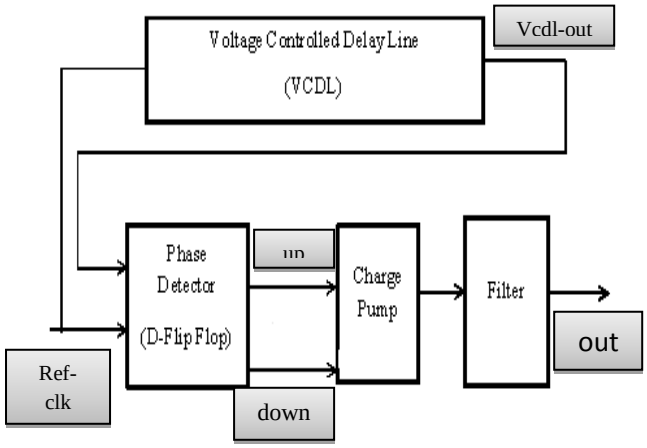

Fig.1. Architecture of DET-DLL Clock Generator

2.1 Voltage Controlled Delay Line (VCDL)

The voltage controlled delay line minimizes the noise accumulation at the output. The VCDL is designed by using current starved inverter model which cascades a set of delay lines. This arrangement minimizes the sensitivity to supply and substrate noise and achieves wide tuning range. The frequency range of the delay line can be increased by changing the delay cells.. The current starved inverter delay model is shown in Fig.2.

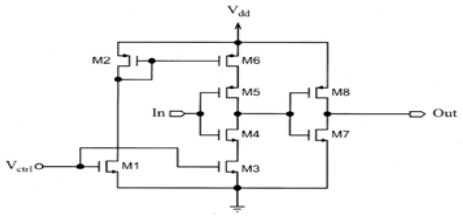

Fig.2 Current Starved Inverter Model of VCDL

The control voltage V_{crl} is applied to series connected element. The single phase clocking scheme reduces the amount of delay added to the circuit.

2.2 Phase Detector (PD)

The phase detector circuit plays a vital role in the DLL clock generator as it detects the phase difference between two input signals. The phase detector is designed using two D-flip flop, one triggers the positive edge and the other triggers the negative edge of the clock pulse, the reference clock (ref_clk) and VCDL signal (VCDL_out) which has to be compared enters the clock inputs.

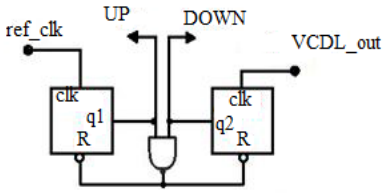

Fig.3 Phase Detector

The two flip flops gives up and down signals which are given to the pulse merging circuit.This merging circuit combines the positive and negative edge pulses. Fig.3 shows the double edge triggered phase detector.

2.2 Charge Pump and Filter

The basic charge-pump loop filter consists of a charge-up as well as a discharge path accompanying with a capacitor to configure the low pass filtering function. It is controlled by the output of the phase detector and either charges or discharges to a voltage level to control the oscillating frequency of VCO. As shown on Fig.4 the switch S1 works for the charging path and the switch S2 is for discharging use.

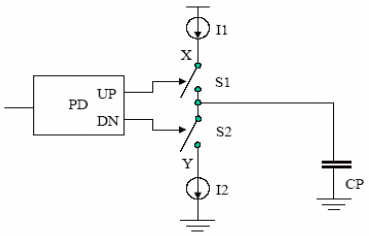

Fig.4 Charge pump and Filter

3. SIMULATION RESULTS

The clock generator is designed using Single Edge Triggering (SET-DLL) and Double Edge Triggering (DET_DLL). The schematic and output of SET-DLL is shown in Fig.5 and Fig.6

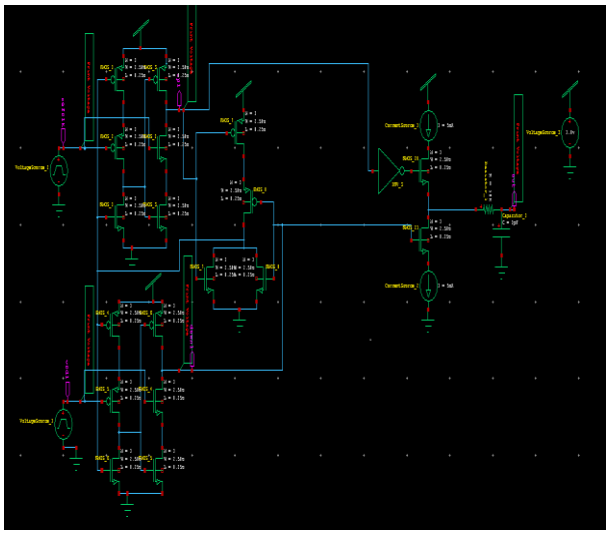

Fig.5 Schematic of SET-DLL clock generator

The schematic of the SET-DLL (positive edge triggered) is designed using truly single phase clocking scheme. The OR gate is used to reset the flip flop. The output of the VCDL line leads the ref_clk thus the up signal will be triggered.

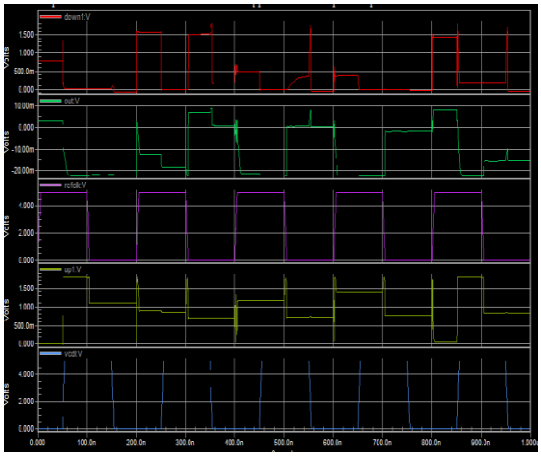

Fig.5 Output of SET-DLL (positive edge)

The SET-DLL suffers from a narrow range and bandwidth. To overcome this issue double edge triggered DLL is designed and the design is shown in Fig.6.

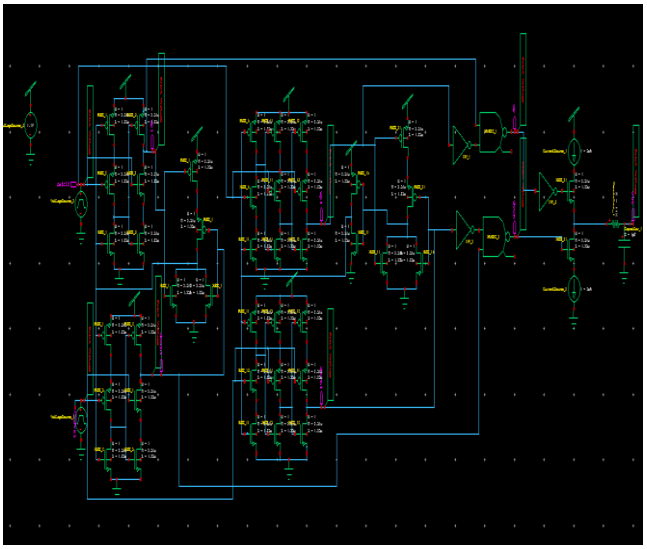

Fig.6 Schematic of DET-DLL clock generator

The design of DET-DLL is made by combining the positive edge triggering and negative edge triggering circuit. The merging circuit uses NAND gate design for combining both the positive and negative pulses. The DET-DLL has a wide bandwidth and it has accurate locking characteristics. The output of the DET-DLL is shown in the Fig.7

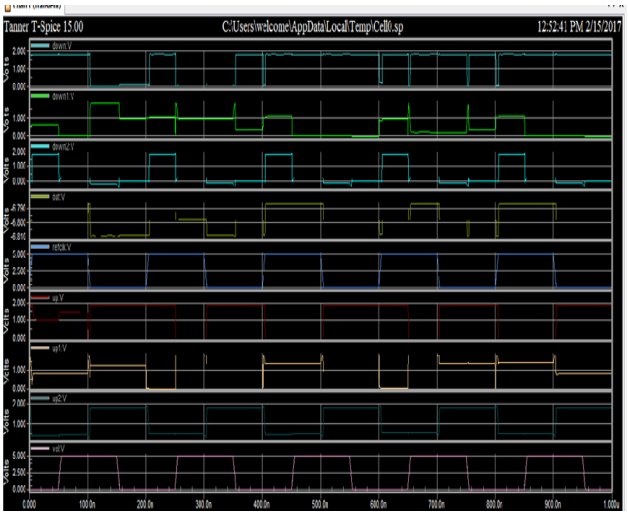

Fig.7 Output of DET-DLL

4. RESULT

The proposed DET-DLL is simulated using 180nm and 65nm CMOS process and the power is compared between SET-DLL and DET-DLL. The design operates at a frequency of 800MHZ with a supply voltage of 1.8V. The power analysis is shown in the Table 1.

Table no. 1. Comparison of power consumed by SET-DLL and DET-DLL

CMOS Process	Power Consumed by SET-DLL	Power consumed by DET-DLL	Frequency
180nm	8.293mW	6.29mW	500MHZ
65nm	5.328mW	3.43mW	500MHZ

It is found that as the technology decreases the power consumption decreases. Thus the power consumed by DET-DLL decreases by 10% compared to SET-DLL.

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